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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,895	08/29/2003	Peter Fricke	10018228-4	8691

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,895	FRICKE ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *72-141* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *72-123 and 125-141* is/are rejected.

7)☒ Claim(s) *124* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/6/03 & 1/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Preliminary Amendment

1. Acknowledgment is made of applicant's Preliminary Amendment, filed 29 August 2003. The changes and remarks disclosed therein were considered.

Claims 1-71 have been cancelled, and claims 72-141 have been added. Therefore, claims 72-141 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 06 October 2003 and 16 January 2004. The information disclosed therein was considered.

Specification, Priority

3. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 as follows:

An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any prior nonprovisional application must include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 132-141 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 132 recites the limitation "the vertical bit lines" in line 9 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 133 recites the limitation "a substrate." It is unclear whether this limitation is same as that recited in the parent claim 132. It will be understood as being the same.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 72, 82, 92 and 122 are rejected under 35 U.S.C. 102(a) as being anticipated by Toyama (European Pat. Appl. Pub. No. EP 0073486 A2).

Regarding claims 72, 82, 92 and 122, Toyama, for example in Figs. 1-3, discloses a cubic memory comprising a substrate (10a; see also page 5 line 12), a plurality of levels of memory cells (levels 12a-12d), a plurality of sets of first select lines in planes parallel to the substrate (or horizontal select lines or word lines) (for example, word lines w11, w21 and w31 in plane 12d), a

plurality of sets of second lines in planes orthogonal to the substrate (or vertical select lines or vertical bit lines) (for example, bit lines B11 and B21 in a vertical plane), wherein each memory cell is adjacent to a respective first and second select line (for example, cell M111 adjacent to word line w11 and bit line B11 in Figs. 1-3).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 81, 91, 101, 102, 111, 112 and 121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyama (European Pat. Appl. Pub. No. EP 0073486 A2).

Regarding claims 81, 91, 101, 102, 111, 112 and 121, Toyama discloses a cubic memory array as in claims 72, 82, 92 and 122 above, and further discloses an array of sub-pillars forming a vertical select lines (or bit lines) (inherent in order for vertical bit lines to cross the plurality of levels of memory cells and insulating layers; see also Fig. 3), with the exception of these sub-pillars connected by a subset of second select lines formed parallel to the substrate surface (or horizonal bit lines).

However, Toyama discloses "parent word lines" (for example, W1 in Fig. 1) connected to a respective set of word lines (for example, w11, w21 and w31) in a horizontal plane, with bit lines individually addressable. Further, in Fig. 4, Toyama discloses another embodiment in which the parent word lines (for example, W1) are connected to a respective set of word lines

(for example, w11, w12, w13 and w14) in a vertical plane, as an alternative equivalent means for addressing a single cell.

Therefore, in view of these variations presented in Toyama, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the cubic memory array of Toyama (Fig. 1) by providing horizontal bit lines (similar to the "parent word lines" of Figs. 1 and 4) connected to a respective set of vertical bit lines (for example, B11 and B21) in a vertical plane and having the word lines individually addressable, since such modification as an alternative equivalent means for addressing a singles cell in the cubic memory array of Toyama (Fig. 1) involves only routine skill in the art.

10. Claims 73-77, 80, 83-87, 90, 93-97, 100, 103-107, 110, 113-117, 120 and 125-129 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyama (European Pat. Appl. Pub. No. EP 0073486 A2).

Regarding claims 73-76, 83-86, 93-96, 103-106, 113-116 and 125-128, Toyama discloses a cubic memory array as in claims 72, 82, 92, 102, 112 and 122 above, with the exception of at least one of the memory cells storing multiple states, or including an antifuse device, a tunnel junction device or a control element having a cross-sectional area greater than a cross-sectional area of a storage device in series. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the structure of Toyama to a memory device type with memory cells storing multiple states (for example, multiple threshold EEPROM cells), or including an antifuse device, a tunnel junction device or a control element having a cross-sectional area greater than a cross-sectional area of a storage device in series (for example, a

memory cell comprising a control diode in series with a fuse), since such memory device types were common and well known in the art, for the purpose of increasing the memory capacity of such memory device types (see for example Toyama page 3 lines 18-20).

Regarding claims 77, 87, 97, 107, 117 and 129, Toyama discloses a cubic memory array as in claims 72, 82, 92, 102, 112 and 122 above, with the exception of the second select lines (or bit lines) formed of tungsten. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to form the second select lines (or bit lines) of Toyama with tungsten, since tungsten was well known in the art and commonly used as an alternative metal for conductors in memory devices.

Regarding claims 80, 90, 100, 110 and 120, Toyama discloses a cubic memory array as in claims 72, 82, 92, 102 and 112 above, with the exception of the first select lines (or word lines) formed in at least a partial serpentine pattern. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have a serpentine (or zigzag) pattern for the first select lines (or word lines) of Toyama, since such pattern was well known in the art to reduce coupling between lines in a high density memory devices.

11. Claims 78, 79, 88, 89, 98, 99, 108, 109, 118, 119, 130 and 131 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyama (European Pat. Appl. Pub. No. EP 0073486 A2) in view of Kubota (U.S. Pat. No. 5,191,550).

Regarding claims 78, 79, 88, 89, 98, 99, 108, 109, 118, 119, 130 and 131, Toyama discloses a cubic memory array as in claims 72, 82, 92, 102, 112 and 122 above, with the exception of at least one of the memory cells including an angled storage element or having a dual storage elements wherein only one storage element is used. Kubota discloses a memory cell including an angled storage device (for example, angled antifuse layer 12 or 22 in Fig. 2) and having a dual storage elements (for example, 10 and 20 of Figs. 1 and 2) wherein only one storage elements is used (see for example column 4, lines 26-30). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the structure of Toyama to the dual antifuse memory device of Kubota, for the purpose of increasing the memory capacity of such memory device type (see for example Toyama page 3 lines 18-20).

12. Claim 123 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyama (European Pat. Appl. Pub. No. EP 0073486 A2) in view of Johnson et al. (U.S. Pat. No. 6,185,122).

Regarding claim 123, Toyama discloses a cubic memory array as in claim 122 above, with the exception of a control circuitry in the substrate including a set of control elements connected to a respective vertical select line. Johnson discloses that the control circuitry formed in the substrate. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have a control circuitry in the substrate of Toyama and include a set of control elements connected to a respective vertical select line, for the purpose of effectively integrating the control circuitry with the cubic memory cells.

Allowable Subject Matter

13. Claim 124 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 132-141 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

15. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 124, the prior arts of record do not disclose or suggest a cubic memory comprising control elements dispose on top of the vertical select lines and a set of horizontal bit lines connecting the control elements to the control circuitry.

Regarding claim 132, the prior arts of record do not disclose or suggest a cubic memory array comprising vertical bit lines that are formed in more than one pillar and are interconnected by one of the set of top sub-column connects and one of the set of bottom sub-column connects, wherein the every other pillar is connected one of a top sub-column connect or a bottom sub-column connect.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Butz (U.S. Pat. No. 6,462,977) discloses a three dimensional memory.

Look et al. (U.S. Pat. No. 5,475,253) discloses an antifuse structure.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800